InGaAs Double-Gate Fin-Sidewall MOSFET

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InGaAs Double-gate MOSFETs with fins as narrow as 12 nm were fabricated using precision dry etching and digital etch. The primary goal is to use the subthreshold characteristics of long-channel devices to characterize the interface of etched InGaAs fin sidewalls. We have investigated the impact of forming gas anneal, high-K oxide and number of digital etch cycles following RIE. Our results indicate a minimum interface state density (D_{it}) of ~$3x10^{12}$ $cm^{-2}eV^{-1}$ obtained in fin sidewalls with Al_2O_3 and HfO_2 oxides after 4 cycles of digital etch. This is equivalent to results reported on planar devices and bodes well for future Trigate MOSFETs that will not require a barrier semiconductor covering the sidewalls.

InGaAs has emerged as the most promising n-channel material for sub-10 nm CMOS [1]. In this dimensional range, only high aspect-ratio 3D transistors with a fin or nanowire configuration can deliver the necessary performance. This brings to the fore the need to achieve high quality MOS interfaces on the sidewalls of these devices, a topic about which little is known. In this work we fabricate double-gate fin MOSFETs and characterize the sidewall MOS interface of dry-etched InGaAs fins through their subthreshold behavior.

The device schematic and process flow are shown in **Fig. 1**. In essence, this is an n-type doped-channel FinFET where the gate only acts on the sidewall surface potential. The starting material consists of a 100 nm thick n-$In_{0.53}Ga_{0.47}As$ active layer Si doped at 10^{18} cm^{-3} on a semi-insulating substrate. A novel reactive-ion etching process that utilizes a $BCl_3/SiCl_4/Ar$ chemistry has been used to define fins as narrow as 20 nm with an aspect ratio of 10 [2]. The fins feature smooth sidewalls that are highly vertical in the top ~70 nm. To further smooth the sidewalls, we perform multiple cycles of digital etch [3]. This consists of a self-limited plasma oxidation/diluted H_2SO_4 sequence that reduces the fin width by ~2 nm per cycle (**Fig. 2**). Three splits with 0, 2 and 4 cycles of digital etch are tested in this work. Immediately after digital etch, the sample is loaded into the ALD for gate dielectric deposition. We separately used 13.5 nm of HfO_2 and 6 nm of Al_2O_3 (both with EOT ~3.7-4 nm). Gating from the top facet of the fin is suppressed by leaving in place the SiO_2 hard mask (>25 nm thick) that was used in their patterning. Sputtered Mo is used as gate metal and patterned by RIE. Evaporated Mo/Ti/Au is used for source and drain contacts and pads. The final step is annealing in forming gas for 30 min at 400C. SEM cross-section of a finished device is shown in **Fig. 3**. A typical device consists of 100 fins, 5 μm in length, with fin widths (W_f) ranging from 10 to 40 nm. The process splits examined in this work are summarized in **Fig 4**.

Output characteristics of a W_f=12 nm device are shown in **Fig. 5**. Well-behaved long-channel characteristics are obtained as a result of good electrostatic control over the fin sidewalls. Subthreshold characteristics for different W_f are shown in **Fig. 6** along with local subthreshold swing, S, and gate leakage. I_{off} is a strong function of fin width. Split CV measurements at 1 MHz were performed (**Fig. 7**) in order to extract carrier mobility (**Fig. 8).** We obtain values that are ~5-7 times lower than expected for the fin doping level. This reveals the importance of sidewall scattering. The drop in mobility for narrow fins also governs the behavior of g_m (inset of **Fig. 8**). **Fig. 9** graphs the minimum subthreshold swing, S_{min}, as a function of W_f for HfO_2 vs. Al_2O_3 before and after anneal. In all cases, S_{min} drops as W_f shrinks. S_{min} greatly improves after annealing. The effect of digital etch is similarly shown in **Fig. 10**. Digital etch appears to significantly improve S in wider fins but not in very narrow fins.

In our doped-channel MOSFETs, once the fin is fully depleted, the ideal value of S is 60 mV/dec. The softer subthreshold characteristics of Fig. 6 reveal the presence of D_{it} on the fin sidewalls. Since fins of different W_f are depleted at a different surface potential, tracing S_{min} as a function of W_f maps the D_{it} distribution across the bandgap. Thicker fins map D_{it} closer to the valence band. This is illustrated in **Fig. 11** that depicts the effect of different D_{it} profiles on S for different W_f. This is obtained from 2D self-consistent Poisson – Schrodinger simulations. From the data of Fig. 9, we can therefore conclude that post-deposition anneal significantly reduces D_{it} across the entire band gap, while digital etch does not affect the minimum D_{it} but impacts its rise towards the valence band with increasing number of cycles reducing D_{it} (Fig. 10). Similarly, Al_2O_3 and HfO_2 may reach the same minimum D_{it}, however, in HfO_2, D_{it} rises faster towards the VB (Fig. 9).

For split 3, using the mobility data, we derived the electron concentration in the fin as a function of gate bias and perform a detailed extraction of D_{it} across the bandgap by comparing with P-S simulations (**Fig 12)**. A U-shape D_{it} distribution emerges that provides excellent agreement with measurements over the entire range of W_f. The D_{it} shape is consistent with previous observations on planar MOSFET structures [4]. A minimum value of ~$3x10^{12}$ $eV^{-1}cm^{-2}$ close to the conduction band edge is obtained. This bodes well for the viability of future Trigate MOSFETs that do not require a wide bandgap semiconductor barrier layer on the sidewalls.

In summary, we demonstrate a new double-gate fin MOSFET to study the interfacial properties of InGaAs sidewalls. Fully operational devices with fin widths as narrow as 12 nm are demonstrated. The combination of RIE and digital etch yields sidewalls with interfacial quality that approaches that of planar surfaces. RIE plus digital etch exhibit clear merit for future sub-10 nm surface-channel InGaAs Trigate MOSFETs.

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References

[1] J. A. del Alamo, *Nature,* 479, 317-323 (2011). [2] X. Zhao *et al., IEDM* 2013, pp. 695-698. [3] J. Lin *et al., IEDM* 2013, pp. 421-424. [4] G. Brammertz *et al., Appl. Phys. Lett.,* 95, 202109 (2009)

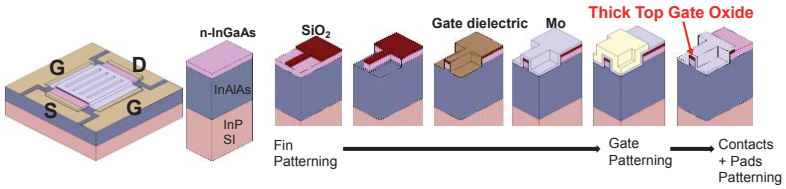


Fig. 1 Device schematic (left) and process flow of double-gate MOSFET.

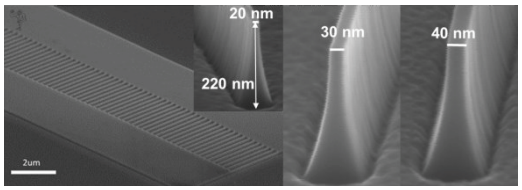


Fig. 2 Device layout (left) and 20 nm fin (inset). 40 nm fin before (right) and after 5 cycles of digital etch (center)

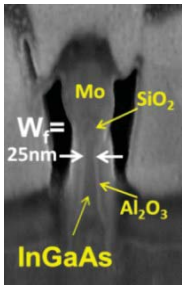


Fig. 3 XSEM of device with 25 nm wide fins.

split	# Digital Etch Cycles	Gate Oxide
1	0	Al_2O_3
2	2	Al_2O_3
3	4	Al_2O_3
4	4	HfO_2

Fig. 4 Process splits examined in this work.

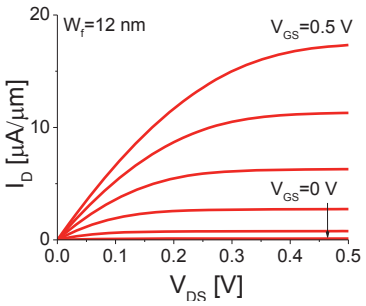


Fig. 5 Output characteristics of double-gate MOSFET with W_f=12 nm (split 3).

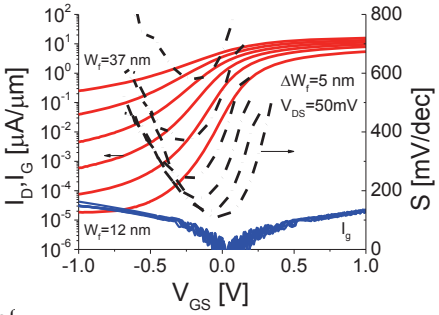


Fig. 6 Subthreshold characteristics, subthreshold swing and gate current for different fin width devices (split 3).

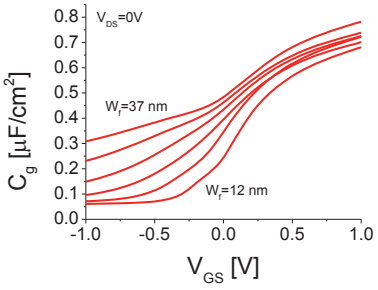


Fig. 7 Split CV measurement of devices with different fin widths (split 3).

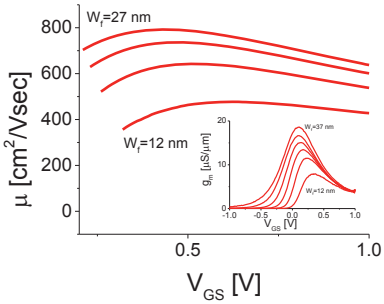


Fig. 8 Channel mobility as extracted from split CV measurements for different W_f. Inset: g_m vs. V_{GS} for different W_f (split 3).

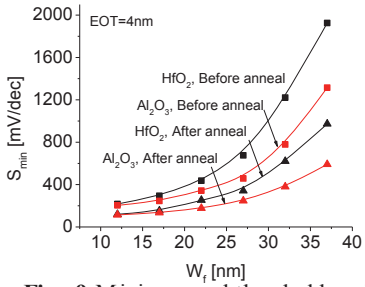
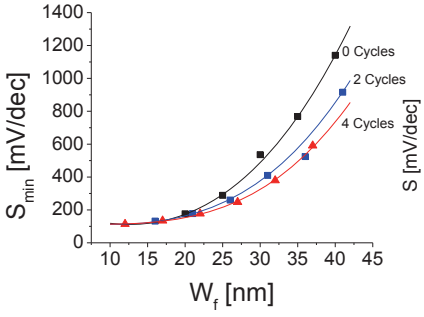


Fig. 9 Minimum subthreshold swing vs. Wf for different dielectrics before and after annealing (splits 3 and 4).



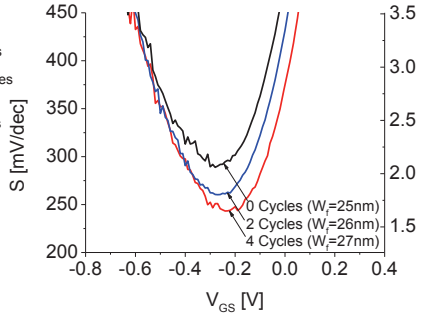


Fig. 10 Left: Minimum subthreshold swing vs. W_f for different digital etch cycles (splits 1-3). Right: effect of digital etch on S (left scale), and the corresponding D_{it} assuming full depletion (right scale) for three devices with W_f~26 nm.

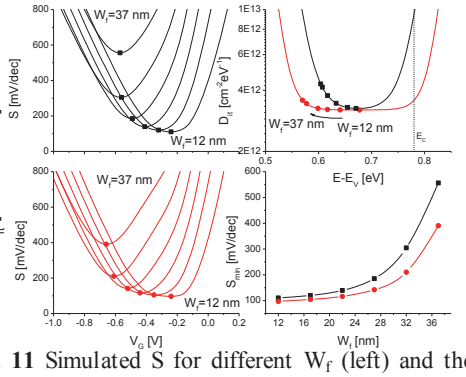
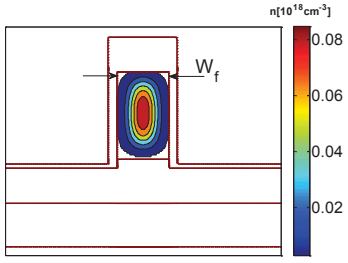
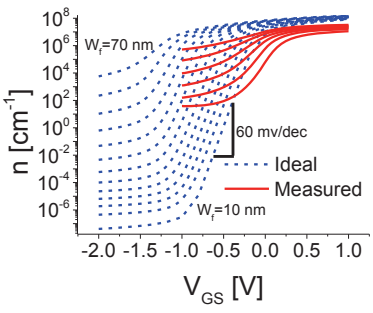


Fig. 11 Simulated S for different W_f (left) and the corresponding S_{min} as a function of W_f (right-down) for two different D_{it} profiles (right-up). S_{min} marked.





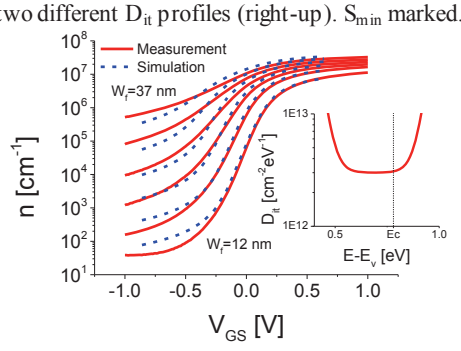


Fig. 12 Comparison between measurement (split 3) and self-consistent 2D Poisson-Schrodinger simulations. Left: simulated structure and electron density at threshold. Center: without D_{it}. Right: with the D_{it} distribution shown in the inset.